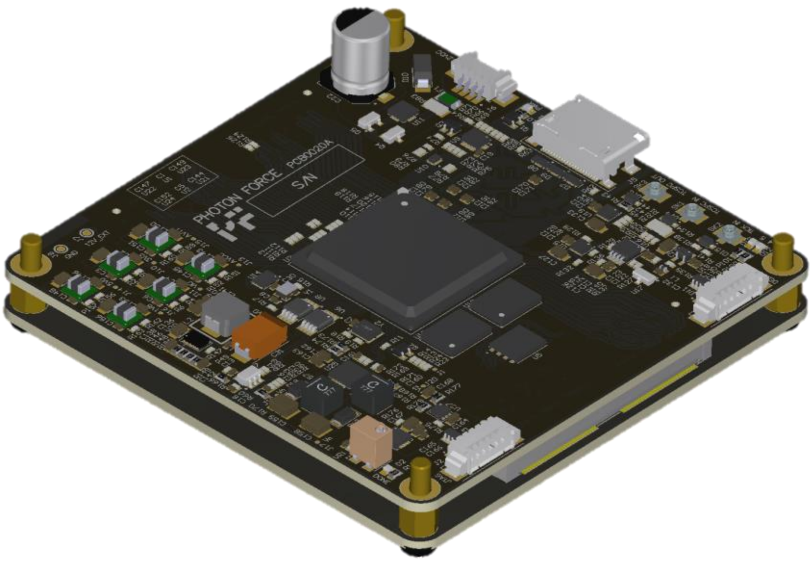
PF32 Module

ACTIVE DEVELOPMENT, April 2024

Rev 0.19



INTRODUCTION

The PF32 sensor consists of 1024 single-photon avalanche diodes (SPADs) arranged in a 32 × 32 array. Each pixel has its own photon counting and timing electronics, making it a powerful and unique single-photon sensitive time-resolved imager. It can be used in time-correlated single-photon counting (TCSPC) mode with a photon timing accuracy of 55 ps, or it can be used in photon counting mode as a single-photon sensitive high frame rate camera. In TCSPC mode, the sensor can be operated in conjunction with a wide variety of light sources, such as pulsed lasers and LEDs, to perform time-resolved measurements. To accommodate the differing properties of these devices, a number of clocking/synchronisation options can be provided. Presented in a compact module form factor, the PF32 Module is ideal for integration into larger systems. The module is designed to communicate with a PC with a PCI Express interface. See host requirements section for further details.

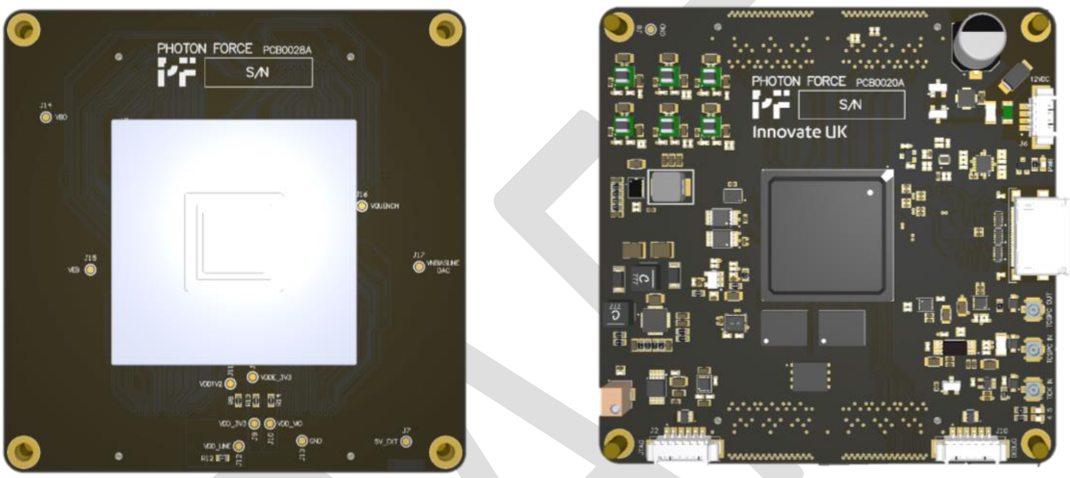


Figure 1: CAD Renderings of Module Boards.

DEFINITIONS

Afterpulsing

SPAD afterpulsing is a phenomenon where delayed pulses are generated after the primary detection event. These secondary pulses are caused by residual charge carriers lingering in the semiconductor material following avalanche breakdown.

Crosstalk

Crosstalk occurs when the firing of one SPAD triggers the firing of an adjacent SPAD with a certain probability, leading to unwanted signal contamination. Within the context of an optical sensor, this can lead to lower effective spatial resolution.

DCR

Dark Count Rate (DCR) in the context of SPADs refers to the rate at which the detector generates electrical pulses in the absence of any incident photons. It measures the intrinsic noise level of the SPAD, typically caused by thermal effects and material defects.

SPAD

A Single Photon Avalanche Diode (SPAD) is a semiconductor device that detects individual photons with extremely high sensitivity. When a photon strikes the SPAD, it triggers an avalanche of charge, resulting in a measurable electrical signal.

SPDE

Single Photon Detection Efficiency (SPDE) measures the probability of accurately detecting individual photons. It accounts for factors such as quantum efficiency and dead time, and dark count rate, providing a quantification of the SPAD's ability to reliably detect single photons against background noise.

TDC

A Time-to-Digital Converter (TDC) is a device that measures the time interval between two events with high precision. It converts the time difference into a digital output, typically in the form of a digital count or timestamp.

FEATURES

EXAMPLE APPLICATIONS

- LiDAR
- Standoff sensing / detection / identification
- Time-resolved fluorescence lifetime spectroscopy
- Time-resolved Raman spectroscopy
- Flow cytometry

KEY BENEFITS

- In-module 1024 bin histogramming capability, with programmable bit-depth.
- 32×32 pixel TCSPC imaging array.
- Fully digital photon counting and time-stamping (no analogue readout noise).
- Pipelined operation: simultaneous data acquisition and readout.
- Flexible readout timing allows an increased frame rate for a subset of pixels or reduced number of counter/TDC bits (LSB first).
- Row and column enable/disable settings to define region of interest.
- External laser synchronisation signal and reference clock inputs to provide TDC stop signal and calibration loop reference frequency.
- Proportionally faster readout frame rate with user-programmable reduced bit depth or region of interest.
- Programmable region of interest.
- User-programmable Per-SPAD enable / disable register bit for region of interest selection or suppression of defective pixels.

KEY SPECIFICATIONS

This section describes the key specifications of the PF32 Module. The specifications is divided into two sections, one specific to the sensor and the other for the module.

SENSOR

Optical

Array Resolution	32 x 32 Pixels
Array Size	1.6mm x 1.6mm
Pixel Pitch	50 µm
Optical fill factor (Without Microlens)	1.5%
Optical fill factor (With Microlens)	>15% (illuminated with collimated light source)
Photodetection Efficiency	Peak 28% at 500nm
DCR	<100Hz for 80% of pixels
Afterpulsing	0.02%
Crosstalk	None
SPAD Quenching Circuitry	Active

Photon Counting Parameters

Dynamic Range (Sensor)	Up to 7 bits
Dynamic Range (FPGA)	Up to 16 bits

TCSPC Parameters

TDC Resolution (Nominal)	55 ps
TDC Dynamic Range	10 bit
TDC Full-Scale	55ps – 57ns
IRF (FWHM)	?? ps

Sensor to FPGA readout

Sensor readout architecture	64 lanes @ 80 MHz
Sensor to FPGA Bandwidth	5.12 Gbps
Module to PC Bandwidth	>14 Gbps (16 Gbps Max theoretical) See connectivity section.
Maximum sensor to firmware frame rate, 10-bit data	0.5 Mfps – 8 Mfps
Inter-frame dead time	<50 ns

MODULE

General

Dimensions (Envelope)	80mm x 80mm x 35mm
Comms / Processing PCB	Companion FPGA for processing and host connectivity
In-Module Processing	Histogramming of sensor data 1024 histogram channels 1024 bins per histogram 8 bit bin depth

Power

Connector	Pico-blade (Molex) MPN 0532610471 Wire to Board Connector
Input Voltage	12V ± 5%
Current consumption (Max)	650mA
Power consumption (Max)	7.8W
Mating cable (300mm)	Molex MPN 0151340403

Connectivity

Connector	Molex MPN 1719820142
Communication Standard	PCI Express (gen 2, x4 lane)
Maximum theoretical bandwidth	16 Gbps
Physical Format	OCuLink Connector (SFF-8611)
Example Cable (1.0m)	Molex MPN 202143-1003
Cable length options	0.3m, 0.7m, 0.5m, 1.0m

Timing Signals

Connector	Molex MPN 0734120114
Connector type	UF.L
TCSPC Output	50 Ohm Single ended Fmax: 200MHz
TCSPC Input	50 Ohm Single ended Option for 50 Ohms termination Fmax: 200MHz
General Purpose Timing Input	Frame Syncronisation input Fmax: 1MHz

INTERFACE DEFINITION

There are a 5 connectors of interest on the module, shown in the image below. All the user connectors are along the right hand side of the FPGA PCB, as shown below.

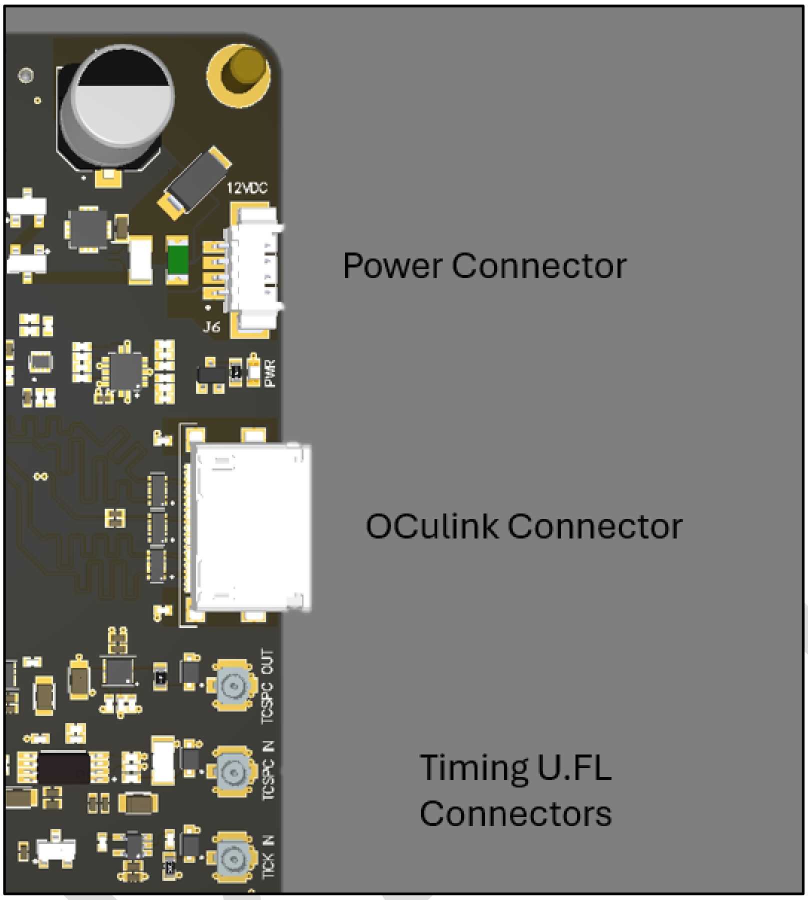


Figure 2: Position of connectors on the FPGA Board.

POWER

The module is designed to take in 12V with a tolerance of 5%. High efficiency DC-DC converters are used to generate all the internal voltages required. The worst case current consumption (max) is 650mA.

The pinout is shown in the table below:

Pin Designator	Net Name
1	GND
2	12V
3	12V
4	GND

DATA

The module is designed to stream data using PCI Express, over an OCuLink cable. The pinout for this connector follows the OCuLink standard, shown below.

Pin Designator	Description	Comment	Pin Designator	Description	Comment
B1	No Connect		A1	No Connect	
B2	Ground		A2	Ground	
B3	PETp0	Module TX	A3	PERp0	Module RX
B4	PETn0	Module TX	A4	PERn0	Module RX
B5	Ground		A5	Ground	
B6	PETp1	Module TX	A6	PERp1	Module RX
B7	PETn1	Module TX	A7	PERn1	Module RX
B8	Ground		A8	Ground	
B9	BP_Type	Module Input	A9	SCL	Reserved
B10	CWAKE	Module Input	A10	SDA	Reserved
B11	Ground		A11	Ground	
B12	CLKp	Module Input	A12	PERST#	Module Input
B13	CLKn	Module Input	A13	CPRSTN#	Module Output
B14	Ground		A14	Ground	
B15	PETp2	Module TX	A15	PERp2	Module RX
B16	PETn2	Module TX	A16	PERn2	Module RX
B17	Ground		A17	Ground	
B18	PETp3	Module TX	A18	PERp3	Module RX
B19	PETn3	Module TX	A19	PERn3	Module RX
B20	Ground		A20	Ground	
B21	No Connect		A21	No Connect	

TIMING SIGNALS

The module has x3 timing signals, described in further detail in the subsections below. All timing signals are:

- Referenced to 3.3V.
- 50 Ohms Characteristic Impedance.

TCSPC IN

This signal is used for TCSPC measurements, where the laser is generating the timing Syncronisation pulses used for the ToF measurement.

TCSPC OUT

This signal can be used as an alternative, when the setup requires the module to generate the timing Syncronisation pulses.

TICK IN

This is a generic timing signal, used to timestamp the frames streamed by the hardware.

HOST REQUIREMENTS

HARDWARE

In order to communicate and control the module, a suitable host machine is required. Below is a list of hardware requirements.

- **PCIe Slot Requirement**
  The host PC must have at least one available PCIe Gen2 x4 slot or higher (Gen 3, Gen 4 slots are backward compatible and could be used, but the operation will be limited to Gen 2 speeds). Using a slot with higher lane count (x8, x16) may also be possible, but the module is limited to x4 lanes. Gen2 at x4 lanes provides 5 GT/s (Giga Transfers per second) per lane, giving a raw 20 GT/s in total. Gen 2 uses a 8/10 bit encoding, which yields a maximum theoretical bandwidth of 16 Gbps.

- **PCIe Form Factor**
  The PCIe slot must be accessible as an OCuLink connector. This can be achieved by either having an OCuLink interface natively on the motherboard, or by using an adapter (PCIe card edge or M.2 to OCuLink connector).

- **Processor**
  The CPU should be capable of handling high-speed data transfers without becoming a bottleneck, including servicing all PCIe lanes in the system without congestion. Typical multicore processors from Intel or AMD from 2019 onwards should be adequate. Lower specifications may also work if lower bandwidths are suitable for the given application.

- **System Memory**
  Adequate RAM is necessary to handle the data throughput and processing requirements. A minimum of 8 GB RAM is recommended, but the specific requirement depends on the end application.

SOFTWARE

The module is provided with a software driver, allowing data streaming and control from the user space, allowing the end application to make method calls via an API.

The API interface is written in ‘C’, but example code is provided to access the module with higher level languages, such as MATLAB or Python.

The software stack provided supports both Linux and Windows.

MICROLENS ARRAY

The PF32 Module can be purchased with a microlens, delivering an overall minimum fill factor of 15%, when illuminated with a collimated light source.

DIMENSIONS

MECHANICAL

The image below illustrates the main dimensions of the module.

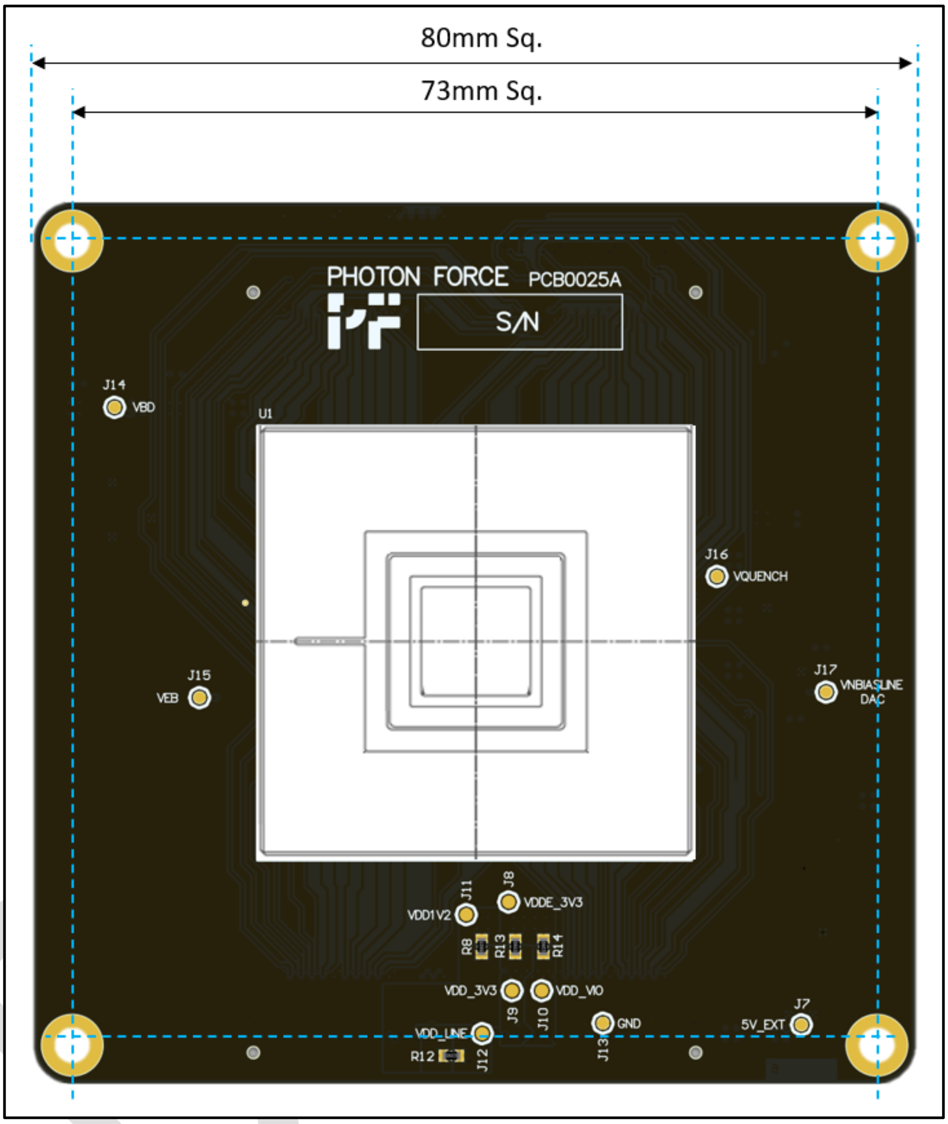


Figure 3: Mechanical Drawing of Module (Top View).

The mounting holes are M3, located symmetrically at 73mm sq. There are also an additional set of 4 holes for mounting a lens, at 30mm sq. The die is located at the centre of the module.

OPTICAL ALIGNMENT

The PF32 sensor (silicon die) has its light sensitive area centred in the middle of the die. From a module perspective, the light sensitive area is at the centre of the mounting holes.

SENSOR OPERATION

SINGLE PHOTON SENSITIVITY

A Single-Photon Avalanche Diode (SPAD) is a photodiode that has been specifically designed to be operated beyond its reverse breakdown voltage, in the so-called "Geiger mode" (as indicated below). While a conventional photodiode would immediately break down if biased in this region, a SPAD can sit stably in this configuration for a period of time, until disturbed by an incoming photon or other noise source.

When a photon is absorbed within the device, creating an electron-hole pair, the resulting avalanche due to impact ionisation provides a rush of current, easily detectable by the surrounding circuitry. The SPAD therefore provides digital detection of a single photon.

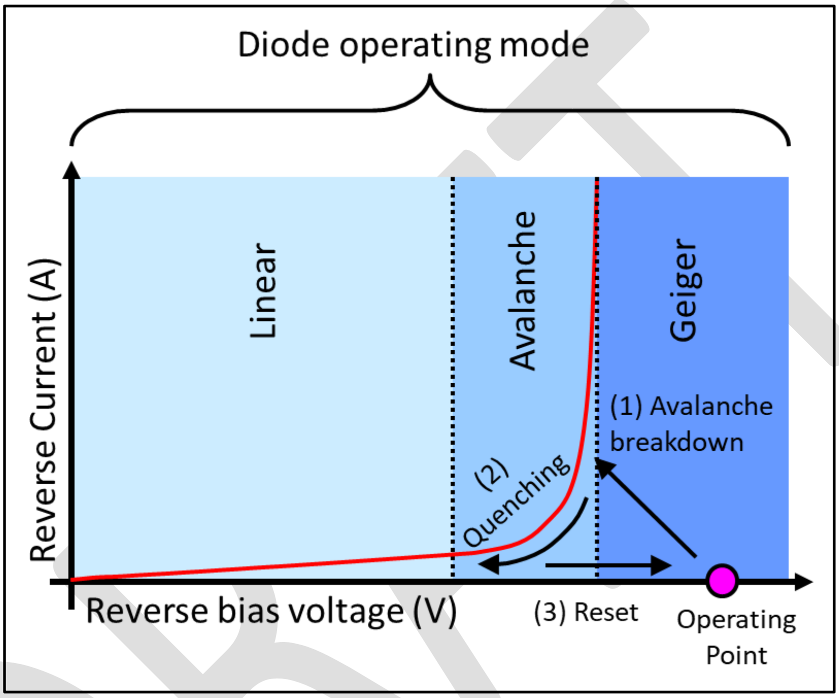


Figure 4: SPAD Operation

PHOTON COUNTING MODE

In photon counting mode, the TDC is configured to simply count the number of photons received during each frame time. No sync is required for the measurement process, making photon counting mode a useful tool for initial setup/alignment of the system before taking TCSPC data. In this mode, each pixel can count multiple photons per frame as shown in the following diagram.

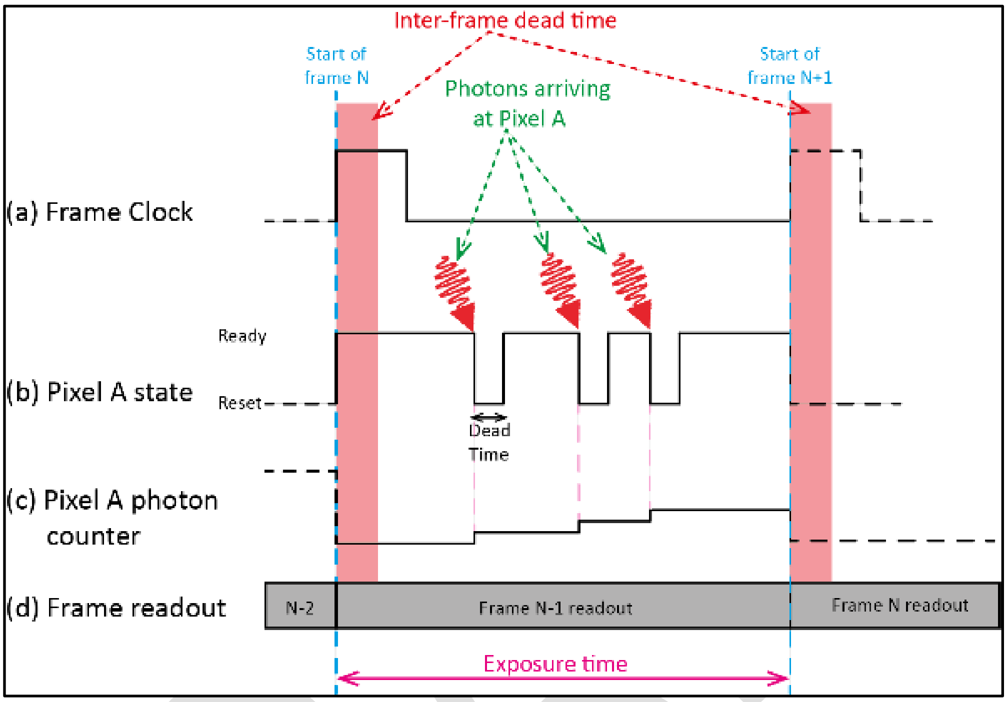


Figure 5: Timing diagram for Photon Counting Mode

TIME-RESOLVED (TCSPC) MODE

TCSPC can be thought of as a fast stopwatch – the start being the emission of the pulsed light source and the stop being the detection of a single photon. However, like many TCSPC systems, the PF32 Module performs reverse start-stop measurements: the detection of a single photon starts the time-to-digital converter (TDC) and the next synchronisation pulse stops this process. This is explained in the following diagram.

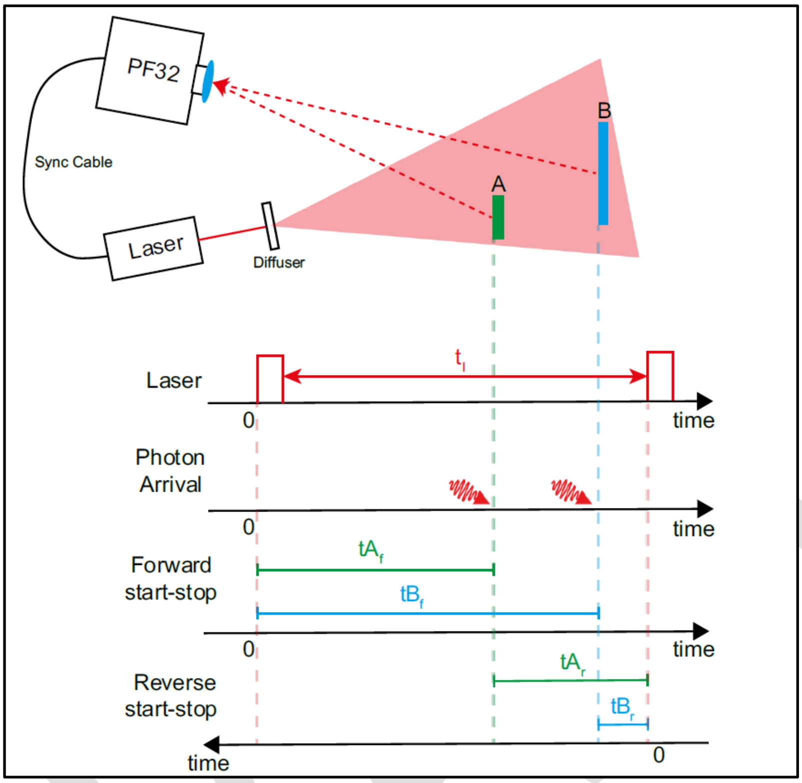


Figure 6: Timing diagram for TCSPC Mode

Reverse start-stop measurements are advantageous since they ensure that the counting electronics are only active when a photon has been detected; in forward start-stop, the synchronisation signal starts the timing and the detection of a photon stops the timing. This means that the timing electronics are in constant use and need to be reset every synchronisation period, potentially increasing readout dead time, power consumption, and heat dissipated through the device.

TCSPC HISTOGRAMMING MODE

In TCSPC histogramming mode, the PF32 Module can timestamp the first photon detected in any given Sync period. The corresponding TCSPC timestamp is streamed to the FPGA, and the pixel becomes available for detection of further photons in subsequent Frame period. A histogram is built within the companion FPGA and made available for readout to the host. Complete TCSPC spectra (comprising number of counts per time bin per micropixel) can then be read out from the module.

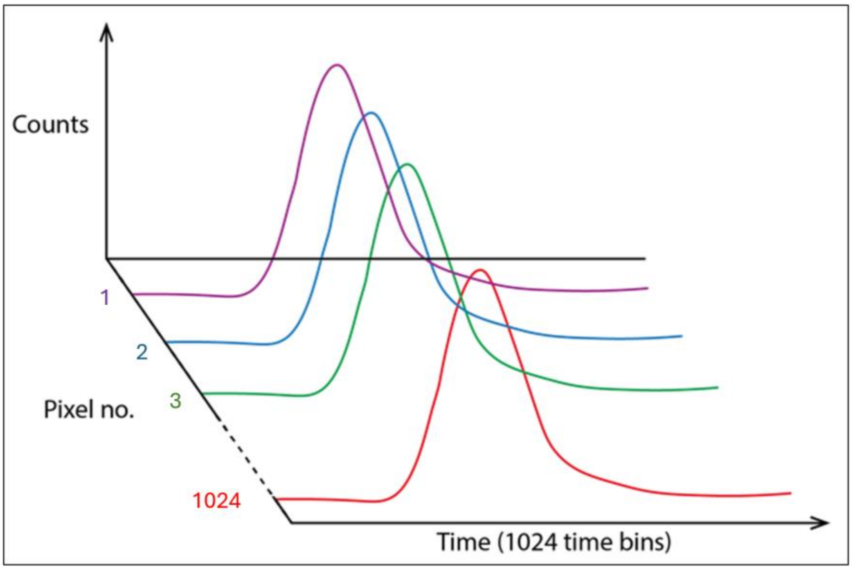


Figure 7: Histogram representation

The bit-depth of the histogram is limited to 8 bits, but can be streamed histograms can be accumulated in the host PC. It is also possible to reduce the number of bins being histogrammed and transmitted to the host PC, reducing the bandwidth requirement on the FPGA to PC Host link.

ULTRA HIGH-SPEED READOUT

The PF32 sensor (silicon die) features a highly flexible ultra-high bandwidth readout system. The data flow originates in the sensor, and is transmitted to the module FPGA via high speed data link. The FPGA streams the data to the host PC via a PCI Express link. This data flow is illustrated in the image below.

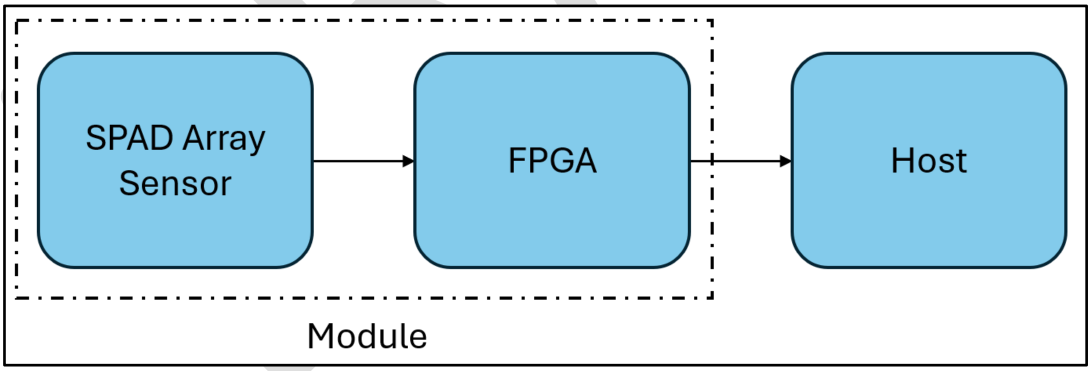


Figure 8: Sensor data flow illustration

The data link between the SPAD Array and the FPGA can provide up to 5.12 Gbps of bandwidth. The PCI Express link can provide up to 16 Gbps.

The high level of configurability in the sensor allows for a trade-off between higher frame rates with reduced number of data bits per pixel (for both Photon Counting / TCSPC mode). It is also possible to read out a subset of the pixels to further increase the maximum frame rate.

EVALUATION KIT

PF32 Module is also available for purchase in camera form for silicon evaluation or scientific/industrial use. This will provide a robust platform for the evaluation of the silicon, utilising the Photon Force software platform.

Figure 9: Example Photon Counting Camera.

CUSTOMISATION

The PF32 Module may be customised to user requirements for volume applications requiring a specific pixel array size, module dimensions or feature set. Please contact Photon Force to discuss your requirements.

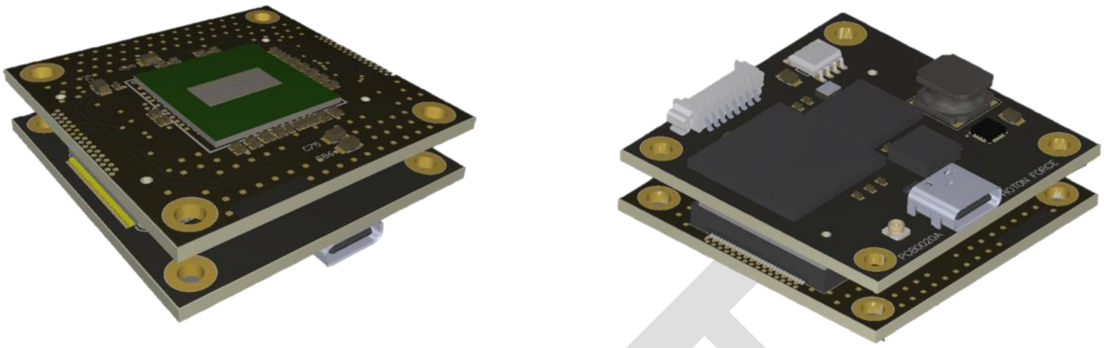


Figure 10: Example Custom Module Designs.

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